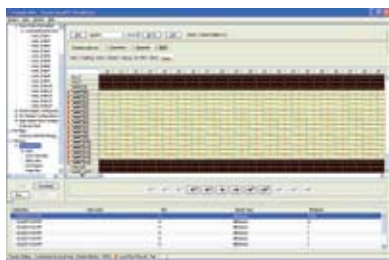




Teseda WorkBench™

Silicon Validation and Diagnostic Software



Diagnose mismatching scan data



Analyze and determine failing trends



Isolate and link to the design level

Leverages your DFT to accelerate real-time, interactive scan validation, IC silicon debug and failure analysis

The **Teseda WorkBench (TWB)** software exploits the full power of your DFT investment, enabling design, test, manufacturing and FA teams to work together to reduce time to production, accelerate yield learning, and maximize profits. The **TWB** operates interactively on the Teseda V5xx series desktop hardware or on your in-house ATE to provide fast, explicit, diagnostic information based on the design and DFT hierarchical information. No more deciphering pin and cycle failure information. Turn days of debug time into hours.

Integrated scan validation graphically identifies problems with scan chains and scan tests for faster diagnosis

The **TWB** software was designed to help you realize the full potential of the DFT that you already use in your devices by integrating with your current tools to perform real-time, interactive scan validation. To speed the initial silicon validation, the **TWB** features integrated scan validation to check the integrity of the physical scan structures and scan patterns, speeding validation and providing accurate failure diagnosis.

Faster, more accurate failure diagnosis through integrated bidirectional communication with EDA scan diagnostic tools

Inside the **TWB**, powerful, graphic-oriented diagnostic tools process actual device test results, design hierarchy and scan-chain structures from IEEE1450 Standard Test Interface Language files generated by DFT tools from Cadence, Mentor Graphics, Synopsys and SynTest. The **Teseda WorkBench** preserves and understands the scan structures generated by your EDA tools and communicates bidirectionally to instantly identify specific problems in a meaningful context for the fastest results so that the scan tools can diagnose failures down to the gate level. The net result is faster, more accurate failure diagnosis.

KEY BENEFITS:

- ▶ Leverages your DFT to accelerate real-time, interactive silicon validation, debug and failure analysis
- ▶ Faster, more accurate failure diagnosis through integrated bidirectional communication with EDA scan diagnostic tools
- ▶ Boosts productivity and supports your work flows with an intuitive graphical user interface and design-based failure information
- ▶ Integrated scan validation graphically identifies problems with scan chains and scan tests for faster diagnosis

Teseda WorkBench™ - Silicon Validation and Diagnostic Software

Boost your productivity with an intuitive graphical interface

The **TWB** features an intuitive, easy-to-use graphical user interface with point-and-click commands - there's no need for long training courses - so your engineers are productive immediately. In addition, the **TWB-Integrator** series also features an Application Programming Interface (API) that supports C++, C, and Java to optimize, automate and integrate your engineering test tasks, boosting your team's productivity, regardless of which programming language or computing environment you are using.

Advanced DFT debug productivity

The **TWB** software graphically displays important information about the location of mismatches detected by your scan chains. You can plot logical defect density spanning all your tests and scan chains and zoom in to get a precise picture of problem areas inside your device. You can zoom in on selected regions, all the way down to individual scan cells, to very quickly determine whether mismatches are evenly spread among the scan cells in a design or concentrated in a region—whether they apply to only a few patterns or the entire pattern set. Powerful graphical utilities can dramatically reduce the time it takes for you to understand and debug mismatches in your scan tests.

Faster, More Accurate Silicon Debug

The **TWB** features views of test results, showing both the scan and design-hierarchy views of information, together with the traditional test vector view, to speed test debug and get new silicon up and running faster, speeding yield ramp-up.

Resolve Test Floor Problems

The **TWB** works with the Teseda V5xx platforms to facilitate design and test collaboration, leveraging design and test views of test results to rapidly determine whether the problem lies in the device or the test program. Resolving test floor problems gets you to higher yield faster.

Faster, More Accurate Failure Analysis

The **TWB** software allows the failure analysis engineer to log test errors in the right format for scan tools to automatically isolate the location of a device defect. This automation accelerates failure analysis, so both design and manufacturing problems causing low yields can be more quickly understood and addressed, increasing profits.

Specifications

Teseda WorkBench for Teseda V5xx

Pattern import/export format:
- STIL (IEEE 1450-1999)

Imported information:

- ▶ Signal names, scan structures, timing, test data

Test data / results views and summaries:

- ▶ Test flow, vector table, scan structure, design hierarchy
- ▶ Failing cycles, failing tests, failing scan chains/cells
- ▶ Shmoo plot, ChainPlot

Workstation Requirements

Host operating system

- ▶ Microsoft Windows 2000 / XP Pro
- ▶ Vista
- ▶ Linux
- ▶ Solaris

1GB RAM minimum

1GHz minimum; 2GHz recommended

20GB available disk space

10/100 Base-T Ethernet

The Teseda V5xx Series™ DFT-Optimized™ Engineering Test Platforms are designed specifically for scan validation and debug, not just as general-purpose testers adapted for DFT test. The hardware is powerful enough for advanced DFT techniques yet is so small and quiet it can sit on your office desktop.



Teseda provides a unifying software and hardware environment that allows multiple engineering disciplines to accelerate the delivery of first silicon.



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